

IN THE CLAIMS:

Please amend claim 5 to read as follows:

5. (Twice Amended) A decoder circuit in (a flash memory device,) comprising:

a global row decoder for outputting a global word line signal; wherein said global row decoder comprises:

a first transistor for transferring a first (voltage) to a node according to a first signal;

a second transistor for transferring a ground voltage to said node according to said first signal;

a third transistor for transferring a second voltage to a global word line according to potential of said node; and

a fourth transistor for transferring said first voltage to said global word line according to potential of said node;

a local row decoder for selecting a word line in response to said global word line signal of said global row decoder, wherein said local row decoder comprises:

a fifth transistor for transferring said global word line signal to said word line in response to a second signal;

a sixth transistor for transferring said global word line signal to said word line according to a third signal; and

a seventh transistor for transferring a ground voltage to said word line in response to said second signal.